What is claimed is:

1. A method for stabilizing data storage for a data-storage memory circuit in a semiconductor device, the memory circuit including a thyristor device having a capacitively-coupled control port and anode and cathode end portions, each end portion including an emitter region and a base region, the capacitively-coupled control port controlled to switch the thyristor device between a current passing mode and a current blocking mode, the method comprising:

shunting low-level current at a first base region of a first one of the end portions.

2. The method of claim 1, wherein said first base region is doped n-type and wherein shunting low-level current includes shunting low-level current between said first base region and another node biased at a voltage at least equal to a voltage at which the adjacent emitter region of said first end portion is biased.

3. The method of claim 1, wherein said first base region is doped p-type and wherein shunting low-level current includes shunting low-level current between said first base region and another node biased at a voltage not greater than a voltage at which the adjacent emitter region of said first end portion is biased.

4. The method of claim 1, wherein shunting low-level current includes coupling a shunt having a low resistance contract to the emitter region of said first end portion and having a comparatively higher resistance contact to the first base region.

5. The method of claim 1, wherein shunting low-level current includes inhibiting the thyristor device from inadvertently switching between current passing and current blocking modes.

6. The method of claim 1, wherein shunting low-level current includes shunting current that could otherwise cause the thyristor device to switch on inadvertently, were the current not shunted.

7. The method of claim 1, further comprising capacitively coupling the control port to a second base region at a second one of the end portions, wherein shunting current includes shunting current at the first base region.

8. The method of claim 1, wherein shunting low-level current includes shunting current between said first base region and an emitter region at the first one of the end portions.

9. The method of claim 1, wherein shunting low-level current includes shunting current between said first base region and a contact electrically coupled to an emitter region adjacent to the first base region.

10. The method of claim 1, wherein shunting low-level current includes shunting tunneling current to the base region.

11. The method of claim 1, wherein shunting current includes resistively coupling an emitter and base region of the anode end portion.

12. The method of claim 1, wherein shunting current includes resistively coupling an emitter and base region of the cathode end portion.

13. The method of claim 1, further comprising providing an intervening region between the first base region and an emitter region at the first one of the end portions.

14. The method of claim 13, further comprising doping the intervening region to a dopant concentration that is higher than the first base region.

15. The method of claim 13, wherein providing an intervening region includes providing a depletion region in the intervening region and wherein shunting current includes shunting current via the depletion region.

16. The method of claim 1, wherein the capacitively-coupled control port is adapted to change the potential across a majority of a cross-section of a base region of the thyristor.

17. A method for stabilizing data storage for a data-storage memory circuit in a semiconductor device, the data-storage memory circuit including an array of thyristors, each thyristor having a capacitively-coupled control port and anode and cathode end

portions, each end portion including an emitter region and a base region, the capacitively-coupled control port being controlled to switch the thyristor between a current passing mode and a current blocking mode, the array being adapted to store data for use in conjunction with the semiconductor device, the method comprising:

shunting low-level current at a first base region of a first one of the end portions of each thyristor.

18. A semiconductor device adapted for stabilizing data storage for a data-storage memory circuit, the semiconductor device comprising:

a thyristor device having a capacitively-coupled control port and anode and cathode end portions, each end portion including an emitter region and a base region, the capacitively-coupled control port controlled to switch the thyristor device between a current passing mode and a current blocking mode; and

means for shunting low-level current at a first base region of a first one of the end portions.

19. A semiconductor device adapted for stabilizing data storage for a data-storage memory circuit, the semiconductor device comprising:

a thyristor device having a capacitively-coupled control port and anode and cathode end portions, each end portion including an emitter region and a base region, the capacitively-coupled control port controlled to switch the thyristor device between a current passing mode and a current blocking mode; and

a low-level current shunt adapted to shunt current at a first base region of a first one of the end portions.

20. The semiconductor device of claim 19, wherein the low-level current shunt includes a transistor having source and drain regions, one of the source and drain regions being electrically coupled to the emitter region of an end portion of the thyristor device and the other of the source and drain regions being electrically coupled to the base region of the same end portion of the thyristor device, the transistor further having a gate adapted to control the current flow between the source and drain regions.

21. The semiconductor device of claim 20, wherein the gate is electrically coupled to a base region of another end portion of the thyristor device.

22. A method for manufacturing a semiconductor device adapted for stabilizing data storage for a data-storage memory circuit, the method comprising:

forming a thyristor device having a capacitively-coupled control port and anode and cathode end portions, each end portion including an emitter region and a base region, the capacitively-coupled control port controlled to switch the thyristor device between a current passing mode and a current blocking mode; and

forming a low-level current shunt adapted to shunt current at a first base region of a first one of the end portions.

23. The method of claim 22, wherein forming a thyristor device includes doping the first base region to n-type doping and wherein forming a low-level current shunt includes forming the low-level current between the first base region and another node biased at a voltage at least equal to a voltage at which the adjacent emitter region of the first end portion is biased.

24. The method of claim 22, wherein forming a thyristor device includes doping the first base region of a first end portion of the thyristor device to p-type doping and wherein forming a low-level current shunt includes forming the low-level current shunt between the first base region and another node biased at a voltage not greater than a voltage at which the adjacent emitter region of the first end portion is biased.

25. The method of claim 22, wherein forming a low-level current shunt includes coupling a shunt having a low resistance contract to the emitter region of the first end portion of the thyristor device and having a comparatively higher resistance contact to the first base region.

26. The method of claim 22, wherein forming a thyristor device includes forming the control port capacitively coupled to a second base region at a second one of the end portions.

27. The method of claim 22, wherein forming a low-level current shunt includes forming the current shunt between the first base region and an emitter region at the first one of the end portions.

28. The method of claim 22, further comprising forming an intervening region between the first base region and an emitter region at the first one of the end portions.

29. The method of claim 28, further comprising doping the intervening region to a dopant concentration that is higher than the dopant concentration of the first base region.

30. The method of claim 28, wherein forming an intervening region includes forming a depletion region in the intervening region and wherein forming a current shunt includes forming a current shunt adapted to shunt current via the depletion region.

31. The method of claim 22, wherein forming a thyristor device includes forming a region having a low effective minority-carrier lifetime, the region at least including a base-emitter junction of the first one of the end portions of the thyristor.

32. The method of claim 31, wherein forming a region having a low effective minority-carrier lifetime includes forming a region having at least one of: poly-crystalline, amorphous, or re-crystallized material.

33. The method of claim 32, wherein forming a region having a low effective minority-carrier lifetime includes creating crystalline damage in the region.

34. The method of claim 31, wherein forming a region having a low effective carrier lifetime includes introducing impurities that lower the lifetime into the region.